Curriculum Vitae

B. Earl Wells Professor Department of Electrical and Computer Engineering College of Engineering University of Alabama in Huntsville Huntsville, AL 35899

Career Objective:

Phone (256) 824-6047 FAX (256) 824-6803 Home (256) 882-6603 email wellsbe@uah.edu

To instruct and lead the research activities of graduate and undergraduate students in the areas of computer and electrical engineering. To conduct relevant research in computer and electrical engineering with specific emphasis on the areas of multi-core and clustered processing, GPU-accelerated and reconfigurable computing, computer simulation, and real- time embedded systems.

Education:

Ph.D. Degree in Electrical Engineering from The University of Alabama Graduation Date: May 9, 1992 Specialization: Computer Engineering Dissertation: "Parallel Simulation Methodologies for Real-Time and Deterministic Systems" Graduate Advisor: Chester C. Carroll

M.S.E.E. Degree from The University of Alabama Graduation Date: May 14, 1988 Specialization: Computer Architecture Thesis: "An Intelligent Processing Environment for Real-Time Simulation" Graduate Advisor: Chester C. Carroll

B.S.E.E. Degree from The University of Alabama Graduation Date: May 14, 1983 Specialization: Digital Systems Honoraries: Tau Beta Pi, Eta Kappa Nu, Alpha Lambda Delta

Registration:

Registered Professional Engineer in the State of Alabama, U.S.A.

Employment History:

5/05 to present -- Interim Chair ECE Department UAH 9/05 to present -- Professor, University of Alabama in Huntsville

10/98 to 8/05-- Associate Professor, University of Alabama in Huntsville 9/92 to 10/98 -- Assistant Professor, University of Alabama in Huntsville 5/92 to 9/92 -- Postdoctoral Research Associate, University of Alabama (Tuscaloosa) 6/88 to 5/92 -- Graduate Teaching/Research Assistant, University of Alabama (Tuscaloosa) 6/84 to 1/87 -- Engineer, Harris Corporation, Palm Bay, Florida

Vitae Outline:

Teaching Activities

Teaching Philosophy

My role as a mentor of Ph.D. and Masters level graduate students is to enable them to success- fully pursue research areas that are consistent with my own. In this mentoring process, I have involved my students in my own research and have incorporated relevant

segments of this research into the classroom. My goal is to produce researchers that are capable of functioning well in academic, industrial, governmental and technical policy making environments.

My role as a college-level instructor of undergraduate students is not simply to train the next generation of technologists, but rather to produce truly *educated* engineers who can advance the state-of-the-art in their discipline while continuously adapting to an ever changing technical landscape. To accomplish this goal, I believe that there should be an appropriate balance between theory and practice -- the ability to view things in a general and abstract manner should be com- plemented by the hands-on experience gained by solving specific, nontrivial real world engineer- ing problems. While it is true that not all engineering courses should have a hands-on component, I have made a special effort to identify courses where integrating such a component contributes to this desired balance. In these courses, I have striven to integrate the theoretical material presented in classes with customized laboratory design work that I have developed. I have also taught the Computer Engineering Capstone Design Sequence for eleven years and numerous special topics courses that allow students to apply the knowledge gained in their undergraduate classes to solve sizable real world problems that are often mult-disciplinary in nature.

Graduate Student Direction:

Ph.D. Graduates (Committee Chair)

Swathi Gurumani "Energy-Efficient Dynamic Task Scheduling Algorithms for Reconfigurable System-

on-chip Architectures," December 2007.

Zexin Pan Dissertation Title: "Hardware Supported Task

Scheduling on Dynamically

Reconfigurable SOC Architectures," May 2006. Yahya Tashtoush

Dissertation Title: "Applying Fuzzy Logic and Reinforcement Learning to Track a Mobile Target using a Wireless Sensor Network," May 2006.

Sin Ming Loo, Dissertation Title: "Static Scheduling in a Reconfigurable Environment," May 2003. Current Position: Professor, Electrical and Computer Engineering Department, Boise

State University, Idaho, U.S.A. Hamid Naji

Dissertation Title: "Agent-Based Reconfigurable Systems," May 2003. Current Position: Dean, College of Electrical & Computer Engineering, Graduate

University of Advanced Technology, Iran. Kenneth G. Ricks,

Dissertation Title: "A Framework for the Design and Specification of Hard Real- Time, Hardware-in-the-loop Simulations for Large, Avionics Systems," August 2002.

Current Position: Associate Professor, ECE Department, University of Alabama (Tuscaloosa), U.S.A.

Ph.D. Graduates (Committee Chair) continued

Abdelrazek Abdelmageed Elsadek Dissertation Title: "New Functional and Data Parallel Methodologies for the Efficient

Distributed Processing of Large-Scale Applications," August 1997. Current Position: Computer and Communication Researcher -- Egyptian Cabinet Information and Decision Support Center (IDSC); Visiting Assistant Professor --The Arab Academy

for Science & Technology and Maritime Transport, Egypt Saleh Hosni Al-Sharaeh

Dissertation Title: “A Massively Parallel Particle-in-Cell Technique for a Three Dimensional Simulation of Plasma Phenomena,” December 1996.

Current Position: Professor, Computer Science, University of Jordan

Thesis Option Master Degree Graduates (Committee Chair)

Stephen Sewell Thesis Title: “Efficient Particle-in-Cell Simulation of Aural Plasma Phenomena using a Cuda

Enabled Graphics Processing Unit”, May 2014. Scott Tashakkor

Thesis Title : “Classification of the use of Polling and Interrupts on Modern Computers“, May 2014.

Jessica Mintz Thesis Title: “A Hardware Implementation of a Traveling Salesman Problem Using a Genetic

Algorithm with Migration,” August 2013. Tom Scott

Thesis Title: “Empirical Evaluation of Reconfigurable Hardware for RFID Applications,” December 2008.

Michael Karle Thesis Title “Software Inspired Hardware Design for Radar Applications,” May 2006.

Swathi Gurumani Thesis Title: “An Intellectual Property Core to support Communicating Sequential

Processes,” December 2003. Robert Hillman

Thesis Title: "Microprocessor System Design for Small Satellites ," December 2000. Sin Ming Loo

Thesis Title: "Portable Parallel Particle-in-Cell Code ," May 2000. Diana L. Hecht

Thesis Title: “An Adaptable Scheduling Approach for Realtime Applications,” May 2000. Guy Prickett

Thesis Title: "Distributed Architecture for Effective Solid State Power Management," May 1998.

Kenneth G. Ricks Thesis Title “An Improved Bus-Based Multiprocessor Architecture,” May 1997.

James M. Lewis Thesis Title: “Boolean Digital Multiplication,” May 1996.

Nitin N. Thakura Thesis Title: “Cache Coherency -- Introduction to Local Directory Scheme”, December 1995.

Jinen Adenwala Thesis Title, “Design of PC Based Data Acquisition System for Welding Robot and Graphical

User Interface for Data Monitoring/Analysis,” August 1994. 3/19

Current Ph.D. Students (Committee Chair)

David Austin Dissertation Topic: “Grain Packing Non-Deterministic Applications in Limited

Resource Partially Reconfigurable Systems” Abedalmohdi Almomany

Current Background Research: “Trade-off and Future Trend Analysis of GPU and FPGA Accelleration Hardware and Software Technologies”

Josh Derbort Current Background Research: “Analysis of Multi-Core, GPU, and hybrid GPU/CPU

Implementations of Particle-Swarm Optimization Methodologies."

Educational Contracts and Awards:* "CUDA Teaching Center," Aleksandar Milenkovic, **B. Earl Wells**, NVIDA Corporation,

Funding $5,031 GTA Matching Funds and GPU equipment donation, April 2013. **Award Period 4/26/13 -- 4/25/14.**

"Systems Engineering of Unmanned Vehicle," AMCOM, Jorge Aunon, R. Frederick, P. Componation, C. Corsetti, D. Berkowitz, P. Farrington, B. Landrum, R. Norman, D. Utley, **B. Wells**, Funding $15,656.82, **Award Period 3/11/02 -- 9/30/02**

"Systems Engineering of Unmanned Hybrid Vehicle," AMCOM, Robert Frederick, J. Aunon, P. Componation, C. Corsetti, D. Berkowitz, P. Farrington, B. Landrum, R. Norman, D. Utley, **B. Wells**, Funding $44,862.89, **Award Period 3/11/02 -- 9/30/02.**

"An Integrated Environment for Rapid Prototyping," **B. Earl Wells**, Rhonda K. Gaede, Robert G. Lindquist, NSF Instrumentation and Laboratory Improvement/NSF DUE-9751482, Funding $47,150, **Award Period 5/9/97 -- 4/8/00**.

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* PI is listed first followed by Co-PIs

Courses Taught:

Total Number of Courses Offerings Taught: 110 (41 Graduate, 42 Undergraduate, 27 Combined Grad/Undergrad). Total Student Instructed -- Head Count: 2132. Total Estimated Unweighted Credit Hour Production: 5,781.

2014/2015: CPE 322 Digital Hardware Design Fundamentals, CPE 324 Advanced Logic Design Lab, CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, CPE 490 Introduction to GPU Programming, CPE 613 General Purpose GPU Programming.

2013/2014: CPE 322 Digital Hardware Design Fundamentals, CPE 324 Advanced Logic Design Lab, CPE 412/ 512 Parallel Programming, CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, CPE 490 Introduction to GPU Programming, CPE 613 General Purpose GPU Programming. ***2012/2013:*** CPE 322 Digital Hardware Design Fundamentals, CPE 324 Advanced Logic Design Lab, CPE 434/ 435/534 Operating Systems and Operating Systems Laboratory, CPE 490 Introduction to GPU Programming, CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, CPE 612 Parallel Algorithms,

CPE 613 General Purpose GPU Computing,

2011/2012: CPE 412/512 Parallel Programing, CPE 490 GPGPU Computing, CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, CPE 422/522 Advanced Logic Design, CPE 790 GPGPU Computing

2010/2011: CPE 434/435/534 Operating Systems and Operating Systems Laboratory, CPE 412/512 Parallel

Programing, CPE 422/522 Advanced Logic Design, CPE 612 Parallel Algorithms

2009/2010: CPE 434/434/534 Operating Systems and Operating Systems Laboratory, CPE 412/512 Parallel Programing, CPE 422/522 Advanced Logic Design, CPE 790 ST:GPU and SOC Computing

2008/2009: CPE 412/512 Parallel Programing, CPE 422/522 Advanced Logic Design, CPE 690 ST: Hardware Accelerated High Performance SOC Computing

2007/2008: CPE 412/512 Parallel Programing, CPE 631 Advanced Computer Architecture, CPE 422/522

Advanced Logic Design, CPE 323 Embedded Systems

2006/2007: CPE 336/337 Operating Systems and Operating Systems Laboratory, CPE 412/512 Parallel Programing, CPE/EE 422/522 Advanced Logic Design, CPE 612 Parallel Algorithms

2005/2006: CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, CPE 412/512 Parallel Programing, CPE/EE 422/522 Advanced Logic Design, CPE 695 Projects in Computer Engineering

2004/2005: CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, CPE 412/512 Parallel Programing, CPE 612 Parallel Algorithms, CPE 619 Modeling and Analysis of Computer and Communication Systems

2003/2004: Sabbatical Research at NASA MSFC ***2002/2003:*** CPE 495 Senior

Design Laboratory I, CPE 496 Senior Design Laboratory II, EE/CPE 422/522

Advanced Logic Design, CPE 695 Projects in Computer Engineering ***2001/2002:*** CPE 495 Senior Design Laboratory I, CPE 496 Senior Design Laboratory II, EE/CPE 422/522 Advanced Logic Design, CPE 612 Parallel Algorithms, CPE 695 Projects in Computer Engineering ***2000/2001:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, EE/CPE 422 -- EE 502 Advanced Logic Design, CPE 410 ST: Digital Rapid Prototyping Techniques, CPE 510 ST: Advanced Testing Techniques, CPE 610 Parallel Proc of Plasma Applications, CPE 710 ST: Hardware/Software Codesign ***1999/2000:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, CPE 595 Microprocessor Development Systems, CPE 610 ST: Parallel Real-Time Systems, EE 610 ST: Reconfigurable Computing, CPE 610 ST: Data Parallel Processing, CPE 742 Parallel Processing Design ***1998/1999:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, EE/CPE 429/509 Microcomputers, CPE 595 Microprocessor Development Systems, EE 610 ST: Reconfigurable Computing ***1997/1998:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, CPE 542 Parallel Processing, EE/CPE 429/509 Microcomputers, CPE 742 Architectures for Parallel Processing, EE 612 Graduate Design Project ***1996/1997:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, CPE 542 Parallel Processing, CPE 602 Digital Computer Design, CPE 610/CPE 710 Special Topics ***1995/1996:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, CPE 542 Parallel Processing, EE 410 Special Topics Hybrid Rocket Class, CPE 610 Special Topics ***1994/1995:*** CPE 427 Senior Design Laboratory I, CPE 437 Senior Design Laboratory II, EE 429/509 Microcomputers, CPE 542 Parallel Processing, EE 610 Special Topics, CPE 631 Architectures for Parallel Processing ***1993/1994:*** EE 410 Special Topics, EE 412 Senior Project, EE 429/509 Microcomputers, CPE 542 Parallel Processing, EE 610 Special Topics, CPE 631 Architectures for Parallel Processing

1992/1993 EE 201 Digital Logic Design Laboratory, EE 429/509 Microcomputers, CPE 542 Parallel Processing, EE 610 Special Topics, EE 612 Graduate Design Project

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Research Activities

Research Focus:

My major area of research is parallel and distributed processing.

This broad area is concerned with partitioning an application problem into sets of operations in which each set of opera- tions can be executed concurrently by different processing engines. The goal of parallel pro- cessing is to improve performance, assure real time execution, increase fault tolerance, improve reliability, and/or decrease power consumption. Parallelization of a given application can be primarily a software problem, when multiple general purpose or embedded processors are interconnected to each other, or such parallelism can be implemented directly within the digital hardware. This hardware itself can be fixed in nature or its low level circuit functional- ity can be configured (and possibly reconfigured) after the physical hardware has been fabri- cated. My contributions to the parallel processing area span this entire software/hardware continuum.

Journal and Book Chapter Publications:

[J.26] "Physical processe in an electron current layer causing intense plasma heating and formation of x-lines" Nagendra Singh, Igor Khazanov, and **B. Earl Wells**, *Physics of Plasmas*, Vol. 22, pp. 052117, 2015.

[J.25] "Rule-based multiple-target tracking in acoustic wireless sensor networks," Young- won Kim An, Seong-Moo Yoo Changhyuk An, and **B. Earl Wells**, *Computer Communi- cations*, Vol. 51, pp. 81-94, 2014.

[J.24] "Doppler effect on target tracking in wireless sensor networks," Youngwon Kim An, Seong-Moo Yoo Changhyuk An, and **B. Earl Wells**, *Computer Communications*, Vol. 36, 2013.

[J.23] "Noise Mitigation for Target Tracking in Wireless Acoustic Sensor Networks," Youngwon Kim An, Seong-Moo Yoo, Changhyuk An, **Earl Wells**, KSII Transactions on Internet and Information Systems, pp. 1166-1179, Vol. 7, No. 5, May. 2013.

[J.22] "Anomalous Resistivity in Reconnecting Current Sheets,"

Nagendra Singh, **B. Earl Wells**, presentation AGU Fall Meeting, San Francisco, December 3-7, 2012.

Digital Design - Combination Logic, " **B. Earl Wells**, Sin Ming Loo, Chapter 20 - *Indus- trial Electronics Handbook 2nd Edition*, CRC press, 2011.

[J. 21] "Features of electron current layers: Comparison between three-dimensional parti- cle-in-cell simulations and Cluster observations", Nagendra Singh, Manish Yeladandi, Tri- nath Somarothu, **B. E. Wells**, *Journal of Geophysical Research*, Vol. 115, 12 pp., 2010.

[J.20] Parallel electric fields in mixing hot and cold plasmas in the auroral downward cur- rent region: Double layers and ambipolar fields, Nagendra Singh, Kalyan Arcot, and B. E. Wells, *Journal of Geophysical Research*, Vol. 114, March 2009.

[J.19] "Hardware Supported Task Scheduling on Dynamically Reconfigurable SoC Archi- tectures", Zexin Pan and **B. Earl Wells**, *IEEE Transactions on VLSI Systems*, Vol. 16, No. 11, November 2008.

[J.18] "Guidelines for Unified System Specification for Co-Design of Embedded Sys- tems," Kenneth G. Ricks, D. Jeff Jackson, **B. Earl Wells**, *The International Journal of Computers and Their Applications*, Vol. 13, No. 3, pp. 128-141, September 2006.

Journal Publications (continued):

[J.17] "A Task Scheduling Methodology within Resource Constrained Reconfigurable Hardware Environments," Sin Ming Loo, **B. Earl Wells**, INFORMS *Journal on Comput- ing*, Vol. 18, No. 2, Spring 2006.

[J.16] "Applying Stochastic Static Task Scheduling to a

Reconfigurable Hardware Environ- ment," Sin Ming Loo, and **B. Earl Wells**, *The International Journal of Computers and Their Applications*, Vol. 12, No. 2, June 2005.

[J.15] "Creating An Adaptive Embedded System by Applying Multi Agent Techniques to Reconfigurable Hardware," Hamid R. Naji, **B. Earl Wells**, and Letha Etzkorn, *Future Gen- eration Computer Systems.*Volume 20, Issue 6, pp. 1055-1081, August 2004.

[J.14] "Applying Multi Agent Techniques to Reconfigurable Systems," Hamid R. Naji, Letha Etzkorn, **B. Earl Wells**, *Advances in Engineering Software,* Volume 35, Issue 7, Pages 401-412, July 2004.

[J.13] "SADL: Simulation Architecture Description Language," Kenneth G. Ricks, John M. Weir, and **B. Earl Wells**, *The International Journal of Computers and Their Applications,* Vol. 9, No. 3, pp. 126-138, September 2002.

[J.12] "Task Allocation and Reallocation for Fault Tolerance in Distributed Computing Systems," Abdelmageed Elsadek, Gamal I. Selim, **B. Earl Wells**, *Scientific Bulletin, Ain Shams University, Faculty of Engineering*, Vol. 36, No.4, pp. 445-456, December 31, 2001.

[J.11] "Electron Hole Structure and its Stability Depending on Plasma Magnetization," Nagendra Singh, S. M. Loo, **B. Earl Wells**, *Journal of Geophysical Research*, Vol. 106, No. A10, pp. 21,183--21,198, October 1, 2001.

[J.10] "Evolution of Electron Beam Generated Waves Resulting in Transverse Ion Heating and Filamentation of the Plasma ," N. Singh, S. M. Loo, **B. E. Wells**, G. S. Lakhina , *Jour- nal of Geophysical Research* , Vol. 106, No. A10. pp. 21,165--21,181, October 1, 2001.

[J.9] "Electron Hole as an Antenna Radiating Plasma Waves, "Nagendra Singh, S. M. Loo, **B. Earl Wells**, *Geophysical Research Letters*, Vol. 28, No. 7, pp. 1371-1374, April 1 2001.

[J.8] "Three-Dimensional Structure of Electron Holes Driven by an Electron Beam," Nagendra Singh, S. M. Loo, **B. Earl Wells**, C. Deverapalli, *Geophysical Research Letters*, Vol. 27, No. 16, pp. 2469-2472, August 15, 2000.

[J.7] "A Heuristic Model for Task Allocation in a Heterogeneous Distributed Computing System," A. Abdelmageed Elsadek, **B. Earl Well**s, *The International Journal of Comput- ers and Their Applications*, Vol. 6, No. 1, pp. 1-13, March 1999.

[J.6] "Three Dimensional Kinetic Simulation of Nonlinear Evaluation of Lower Hybrid Pump Waves," Nagendra Singh, **B. Earl Wells**, A. Abdelrazek, S. Al-Sharaeh, and W. C. Leung, *Journal of Geophysical Research*, pp. 9333-9349, 1998.

[J.5] "Parallel Simulation of A Large Scale Aerospace System In A Multicomputer Envi- ronment," **B. Earl Wells**, Kenneth G. Ricks, John M. Weir, *IEEE Transactions on Aero- space and Electronic Systems*, Vol. 33, No. 2, pp. 507-523, April 1997.

[J.4] "Handicapping 'Judges' Some Theory and Practice," J. Neggers, **B. Earl Wells**, *Qual- ity & Quantity International Journal of Methodology*. Vol. 31. No. 2, pp. 173-191, May 1997.

Journal Publications (continued):

[J.3] "Three-Dimensional Numerical Simulation of Ion and Electron Accelerations by Parametric Decay of Fast Lower Hybrid Waves," N. Singh, S. Al-Sharaeh, A. Abdelrazek, W. C. Leung, **B. E. Wells**, *Geophysical Research Letters*, Vol. 23, No. 24, pp. 3663-3667, December 1, 1996.

[J.2] “A Hard Real-Time Static Task Allocation Methodology for Highly-Constrained Mes- sage-Passing Environments,” **B. Earl Wells**, *The International Journal of Computers and Their Applications*, Vol. II, No. 3. pp. 123-136, December 1995.

[J.1] “A Multicomputer Software Interface for Parallel Dynamic System Simulation,” **B. Earl Wells**, S*imulation Journal of the Society for Computer Simulation*, Vol. 65, No. 3, pp. 191-205, September 1995.

Conferences:

[C.68] "Noise Mitigation for Multiple Targets Tracking in Acoustic Wireless Sensor Net- works," Youngwon Kim An, ChangHyuk An, Seong-Moo Yoo, **B. Earl Wells,** peer reviewed paper #1569930201 IEEE Military Communications Conference, Baltimore, MD. October 6-8, 2014.

[C.67] "UAH OnTrack: Precision Navigation System for Research on The Software Safety Issues of Positive Train Control,” Scott Schiavone, Sjohn Chambers, Sunny Patel, Lee Ann Hanback, David J. Coe, Jason Winningham, **B. Earl Wells,** George Petznick, and Jeffrey H. Kulick, *Proceedings of The 2014 World Congress in Computer Science, Computer Engi- neering*, Las Vegas, NV, U.S.A. July 2014.

[C.66] “Heuristically Driven Task Agglomeration in Limited Resource Partially-Reconfig- urable Systems,” David Austin and **B. Earl Wells**, *International Conference on Engineer- ing of Reconfigurable Systems and Algorithms*, Las Vegas, NV U.S.A, July 22-25, 2013.

[C.65] “Applying a Genetic Algorithm to Reconfigurable Hardware using a Traditional HDL Approach” Jessica Mintz and **B. Earl Wells**, University of Alabama in Huntsville, 36th Annual SIAM Southeastern Atlantic Section Conference, University of Alabama in Huntsville, March 24 - 25, 2012.

[C.64] “Space Weather Phenomena Simulation using a Graphics Processing Unit”, Patrick Gilbert, Scotty Bridges, Jason Schansman, Frank Richard, Nagendra Singh, and **B. Earl Wells**, 36th Annual SIAM Southeastern Atlantic Section Conference, University of Ala- bama in Huntsville, March 24 - 25, 2012.

[C.63] “Energy-Efficient Dynamic Task Scheduling Algorithm for Reconfigurable System- on-Chip Architectures,” Swathi T. Gurumani and **B. Earl Wells**, *Conference on Engineer- ing of Reconfigurable Systems and Algorithms*, Las Vegas, U.S.A., June 25-28, 2007.

[C.62] “Dynamic Power Management in Power-Aware Reconfigurable System-On-Chip Architectures,” Swathi T. Gurumani and **B. Earl Wells**, accepted for publication as a regu- lar research paper in the *Proceedings of the 2007 International Conference on Embedded Systems and Applications*, Las Vegas, U.S.A., June 25-28, 2007.

[C.61] “Performance Analysis of Parallel Two-Dimensional PIC-based Simulation of a Mesoscale Auroral Potential Structure,” **B. Earl Wells** (presenter), Chakri Deverapalli, Nagendra Singh, and Kalyan S. Arcot, Poster Presentation, 2006 Huntsville Workshop Out- standing Problems in Geospace Connections Modeling, Nashville, Tennessee. October 4, 2006.

Conferences (continued):

[C.60] “Performance Analysis of Coarse-Grained Parallel Particle Swarm Optimization,” Swathi T. Gurumani, Mathew M. Noel, **B. Earl Wells**, Thomas C. Jannett, *Proceedings of the 19th International Conference on Parallel and Distributed Computing Systems (PDCS- 2006)*, San Francisco, CA, September 20-22, 2006.

[C.59] “Re-configurable Hardware Based Fractal Neural Processor,” A. H. Abou-Ali, S. M. Abd-El-Moetty, **B. Earl Wells**, *Proceedings of the 19th International Conference on Paral- lel and Distributed Computing Systems (PDCS-2006)*, San Francisco, CA, September 20- 22, 2006.

[C.58] “Microarchitecture Support for the Dynamic Scheduling of Task Systems with Data and Control Dependencies on Reconfigurable Architectures,” Zexin Pan, B. Earl Wells, and Juanjo Noguera, *Proceedings of the 2005 Summer Simulation Multiconference* (SPECTS'05) [Winner of a Best Paper Award one of three such awards given out of 169 papers that were accepted for the conference], Philadelphia/Cherry Hill, PA, July 24-26, 2005.

[C.57] “Improved Microarchitecture Support for Dynamic Task Scheduling on Reconfig- urable Architectures,” Zexin Pan, Juanjo Noguera, **B. Earl Wells**, *Proceedings of the 2005 International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA-05),* Las Vegas, Nevada, USA, June 27-30, 2005.

[C.56] “Applying Fuzzy-Reinforcement Learning to Track a Mobile Target using a Wire- less Sensor Network,” Yahya Tahtoush, **B. Earl Wells**, and Thomas C. Jannett, *Proceed- ings of the 2005 International Conference on Wireless Networks (ICWN-05) ,* Las Vegas, Nevada, USA, June 27-30, 2005.

[C.55] “Functional Simulation of a Dynamic Task Scheduler for Reconfigurable System on a Chip Architectures,” Zexin Pan and **B. Earl Wells**, *Proceedings of the 2004 Huntsville Simulation Conference* (HSC), Huntsville, AL, October 2004.

[C.54] “Simulation and Visualization in the Development of an Underwater Distributed Sensor Field,” Thomas C. Jannett, Alan M. Shih, **B. Earl Wells**, Anish Anthony, Shripad Chandrachood,

Parag Joshi, Rajagopalan Kasthurirangan, Mathew Noel, Dilipkumar Vetrivel, and Jason Winningham, *Proceedings of the 2004 Huntsville Simulation Confer- ence* (HSC), Huntsville, AL, October 2004

[C.53] "A Comparison of Two Parallel Particle-in-Cell Methodologies for Dynamic Auroral Plasma Simulation," **B. Earl Wells**, Igor G. Khazanov and Nagendra Singh, made presentation of ongoing research at the Simulation Methodology Section of the *Huntsville Simulation Conference*, Huntsville, AL, October 20, 2004.

[C.52] "Applying a Genetic Algorithm to Reconfigurable Hardware - a Case Study," **B. Earl Wells**, Clint Patrick, Luis Trevino, John Weir and Jim Steincamp, Millitary and Aeospace Applications of Programmable Logic Devices Conference (MAPLD04), posted for electronic dissemination at http://klabs.org/mapld04/program_sessions/session_e.html, Washington, DC, September 8-10, 2004.

[C.51] "Fuzzy Sensor Fusion using Hardware Agents," Hamid Naji and **B. Earl Wells**, Proceedings of the World Automation Congress in Seville, Spain – WAC 2004 June 28, July 1, 2004.

Conferences (continued):

[C.50] "A Novel ROM-less Direct Digital Frequency Synthesizer Based on Chebyshev Polynomial Interpolation," Ashkan Ashrafi, Zexin Pan, Reza Adhami, and **B. Earl Wells**, *Proceedings of the 36th Southeastern Symposium on System Theory* (SSST-2004), Georgia Institute of Technology, Atlanta, Georgia, pp 393-397, March 2004.

[C.49] "Exploiting Fine-Grain Parallelism present within the International Data Encryption Algorithm using a Xilinx FPGA,"

Zexin Pan, Srikanth Venkateswaran, Swathi Tanjore Gurumani, and **B. Earl Wells**, *Proceedings of the 16th International Conference on Paral- lel and Distributed Computing Systems (PDCS-2003)*, Reno, Nevada, USA, August 13 - 15, 2003.

[C.48] "The Application of Software Process Precedence Relationship Formalisms to Con- current Hardware Systems," Kenneth G. Ricks, D. Jeff Jackson, and **B. Earl Wells**, *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 03),* Las Vegas, Nevada, June 23-26, 2003.

[C.47] "An Agent Inspired Reconfigurable Computing Implementation of a Genetic Algo- rithm," John Weir and **B. Earl Wells**, *Proceedings of the International Conference on Par- allel and Distributed Processing Techniques and Applications (PDPTA' 03),* Las Vegas, Nevada, June 23-26, 2003.

[C.46] "A Survey and Analysis of Precedence Relationship Formalisms for Client-Server Systems," Kenneth G. Ricks, D. Jeff Jackson, and **B. Earl Wells**, *Proceedings of the 18th International Conference on Computers and Their Application* (CATA 2003), Honolulu, Hawaii, USA, March 26-28, 2003.

[C.45] "More Accurate Semantics Defining Constraint Combination for Client-Server Sys- tems," Kenneth G. Ricks, D. Jeff Jackson, and **B. Earl Wells**, *Proceedings of the 18th International Conference on Computers and Their Application* (CATA 2003), Honolulu, Hawaii, USA, March 26-28, 2003.

[C.44] "A Genetic Algorithm Approach to Static Task Scheduling in a Reconfigurable Hardware Environment", S. M. Loo, **B. Earl Wells**, J. Winningham, *Proceedings of the 18th International Conference on Computers and Their Application* (CATA 2003), Hono- lulu, Hawaii, USA, March 26-28, 2003.

[C.43] "A Scalable Three-Dimensional Domain Decomposition

Mapping Technique Using MPI," Saleh H. Al-Sharaeh, **B. Earl Wells**, *Proceedings of the 18th International Confer- ence on Computers and Their Application* (CATA 2003), Honolulu, Hawaii, USA, March 26-28, 2003.

[C.42] "Parallel Image Processing with Agent-based Reconfigurable Hardware," Hamid R. Naji, Reza Adhami, Letha Etzkorn, **B. Earl Wells**, *Proceedings of the 15th International Conference on Parallel and Distributed Computing Systems* (PDCS 2002) , Louisville, KY., September 2002

[C.41] "Applying the Multi-Agent Paradigm to Reconfigurable Hardware , A Sensor Fusion Example ," Hamid R. Naji, John Weir, **B. Earl Wells**, *Proceedings of the Second International Work Shop on Intelligent Systems Design and Application* (ISDA2002), Atlanta ,GA, August 2002.

[C.40] "Hardware agents: A New Approach to Support Development and Management of Information Systems," Hamid R. Naji, Letha Etzkorn, **B. Earl Wells**, *Proceedings of the 6th World Multiconference on Systemics, Cybernetics and Informatics*, Orlando, Florida, July 2002.

Conferences (continued):

[C.39] "Hardware Agents," Hamid R. Naji, **B. Earl Wells**, M. Aborizka, *Proceedings of the ISCA 11th International Conference on Intelligent Systems on Emerging Technologies* (ICIS-2002), Boston, MA, July 2002.

[C.38] "International Product Teams for Aerospace System Design," Robert. A. Frederick, Jr., Marie-Sophie Pawlak, D. M. Utley, C. D. Corsetti, **B. E. Wells**, and D. B. Landrum, *Proceedings of the 38th AIAA/ASME/SAE/ASEE Joint Propulsion Conference and Exhibit*, Indianapolis, Indiana, July 7-10, 2002.

[C.37] “Handel C for Rapid Prototyping of VLSI Coprocessors for Real Time Systems ,” S. M. Loo, **B. Earl Wells**, N. Freije, and J. Kulick, *Proceedings of the Southeastern Sympo- sium on System Theory* (SSST-2002), pp. 6-10, Huntsville, AL, March 18-19, 2002.

[C.36] “On Incorporating Multi Agents in Combined Hardware/Software Based Reconfig- urable Systems -- A General Architectural Framework,” Hamid Reza Naji, **B. Earl Wells**, *Proceedings of the Southeastern Symposium on System Theory* (SSST-2002), pp.344-348, Huntsville, AL, March 18-19, 2002.

[C.35] “On the Use of Distributed Reconfigurable Hardware in Launch Control Avionics,” **B. Earl Wells**, Sin Ming Loo, *Proceedings of the 20th Digital Avionics Systems Confer- ence*, [Session 8B Re-usable Launch Vehicles -- Awarded Best Paper of Session], October 14-18, Datona Beach, FL, 2001.

[C.34] “Case Study: On Performing Efficient Highly Parallel Three-Dimensional PIC based Simulations in Constantly Changing Computing Environments,” **B. Earl Wells**, Sin Ming Loo, and Nagendra Singh, *Proceedings of the 2001 Huntsville Simulation Confer- ence* (HSC), Huntsville, AL, October 3-4, 2001.

[C.33] “SADL: Simulation Architecture Description Language,” Kenneth Ricks, John Weir, and **B. Earl Wells**, *Proceedings of the ISCA 14th International Conference on Paral- lel and Distributed Computing Systems* (PDCS-2001) , Dallas, Texas, August 8-10, 2001.

[C.32] “Exploring the Hardware/Software Continuum in a Computer Engineering Cap- stone Design Class using FPGA-based Programmable Logic,” S. M. Loo **B. E. Wells**, R. K. Gaede, *Proceedings of the 2001 International Conference on Microelectronic Sys- tems Education*, Las Vegas, NV, June 17,18, 2001.

[C.31] “An Integrated Facility for Rapid Prototyping,” R. K. Gaede, and **B. Earl Wells**, contributed to presentation made by Dr. Gaede at Session #1526, 2000 ASEE Annual Con- ference, St. Louis, MO, May 2000.

[C.30] “Case Study: A Portable Parallel Particle-in-cell Code Simulation,” Sin Ming Loo, **B. Earl Wells**, Nagendra Singh, and Edith P. Huang, *Proceedings of the International Con- ference on Parallel and Distributed Processing Techniques and Applications* (PDPTA’ 99), Las Vegas, Nevada, July 13-16, 1999.

[C.29] “Case Study: A Portable Parallel Particle-In-Cell Code Simulation on HP Exem- plar,” Sin Ming Loo, **B. Earl Wells**, and W. E. Cohen, Midwest Society for Programming Languages and Systems, April 10, 1999, Purdue University, Indiana, USA.

[C.28] "Parallel Implementations of a Three-Dimensional PIC code Plasma Simulation," A. Abdelmageed Elsadek, Saleh Al-Sharaeh, Safwat Elnahass, Nagendra Singh, and **B. Earl Wells**, *Proceedings of the ISCA 11th International Conference on Parallel and Distributed Computing Systems*, Chicago, IL, September 2-4, 1998.

Conferences (continued):

[C.27] “An Analysis of an Improved Bus-based Multiprocessor Architecture,” Kenneth G. Ricks, and **B. Earl Wells**, full length paper published in *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications* (PDPTA’ 98), Las Vegas, Nevada, July 13-16, 1998.

[C.26] “Three-Dimensional Plasma Phenomena Simulation on a Cray-T3D MPP System, A. Abdelmageed Elsadek, Saleh Al-Sharaeh, **B. Earl Wells**, and Nagendra Singh, full length paper in

Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 98), Las Vegas, Nevada, July 13-16, 1998.

[C.25] "A Dynamic Model for the Distributed Simulation of a Turbojet Engine," C. Tournes and **B. E. Wells**, *Proceedings of 30th IEEE Southeastern Symposium on System Theory*, pp. 125-129, West Virginia University, West Virginia, March 8-10, 1998.

[C.24] "A Pre-Runtime Assisted Approach to Responsive Scheduling Facilitating a Fault- Tolerant Hardware and Software Architecture," Phil Acuff, **B. Earl Wells**, made presenta- tion at Life Cycle Systems Engineering Conference, Redstone Arsenal, November 4, 1997.

[C.23] "Parallel Three-Dimensional Particle-In-Cell Code Simulation on a Cluster of Heter- ogeneous Workstations," A. Abdelmageed Elsadek, Saleh Al-Sharaeh, **B. Earl Wells**, Nagendra Singh, Short Paper in *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 97),* Las Vegas, Nevada, June 30-July 3, 1997.

[C.22] "Applying Parallel Block Predictor-Corrector Methods to Transputer Type Configu- rations," **B. Earl Wells**, Kenneth G. Ricks, full length *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 97),* pp. 937-946, Las Vegas, Nevada, June 30-July 3, 1997.

[C.21] "Applying Parallel and Distributed Processing Techniques to a Tether Dynamics Simulation," **B. Earl Wells**, John Glaese, full length paper in *Proceedings of the Interna- tional Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 97),* pp. 667-673, Las Vegas, Nevada, June 30-July 3, 1997.

[C.20] “A Case Study: In Support of Employing a Transputer-Style Architecture for Avion- ics Mission and Information Processing,” **B. Earl Wells**, Christian Tournes, Lee Young, full length in *Proceedings of the International Conference on Parallel and Distributed Process- ing Techniques and Applications (PDPTA’ 97),*Las Vegas, Nevada, June 30-July 3, 1997.

[C.19] “Upper Stage Rocket Guidance and Control using Discontinuous Reaction Control Thrusters via Sliding Modes,” C. H. Tournes, Y. B. Shtessel, **B. E. Wells**, in *Proceedings of the 1997 American Control Conference*, Albuquerque, NM, June 4-6, 1997.

[C.18] “Massively Parallel 3-Dimensional Particle-in-Cell Plasma Code,” **B. E. Wells**, S. Al-Sharaeh, and N. Singh, made presentation at the *24th IEEE International Conference on Plasma Science*, San Diego, CA, May 20, 1997.

[C.17] “An Optoelectronic Design of the Simultaneous Optical Multiprocessor Exchange Bus,” R. G. Lindquist, J. Kulick, W. E. Cohen, R. K. Gaede, **B. E. Wells**, M. Abushagur, D. Shen, C. Katsinis, S. T. Kowel, in *Proceedings of Photonics West -- Hybrid Monolithic OEICs*, SPIE Proceedings Vol. 3005, San Jose, CA, February 12-14, 1997.

Conferences (continued):

[C.16] “A Three-Dimensional Plasma Phenomena Simulation on a Cluster of Heterogeneous Work Stations Using PVM,” S. Hosni Al-Sharaeh, A. Abdelmageed Elsadek, **B. Earl Wells**, Nagendra Singh, *Proceedings of the ISCA Ninth International Conference on Computer Applications in Industry and Engineering*, Orlando, FL, pp. 23- 26, December 11-13, 1996.

[C.15] “Heuristic Model for Task Allocation in a Heterogeneous

Distributed Computing System" (general handicapping technique), A. Abdelmageed Elsadek, **B. Earl Wells**, *Pro- ceedings of the ISCA Ninth International Conference on Computer Applications in Industry and Engineering*, Orlando, FL, pp. 9-12, December 11-13, 1996.

[C.14] "A Massively Parallel Particle-in-Cell Technique for the Three-Dimensional Simu- lation of Plasma Phenomena," S. Hosni Al-Sharaeh, **B. Earl Wells**, Nagendra Singh, *Pro- ceedings of the ISCA Ninth International Conference on Parallel and Distributed Computing Systems (PDCS)*, Dijon, France, September 25-27, 1996.

[C.13] "Heuristic Model for Task Allocation in a Heterogeneous Distributed Computing System," A. Abdelmageed Elsadek, **B. Earl Wells**, *Proceedings of the International Con- ference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 96),* Sunnyvale Hilton, California, pp. 659-670, August 9-11, 1996.

[C.12] "A Comparison of Heuristics for List Schedules using the Box-Method and P- Method for Random Digraph Generation," Saleh Al-Sharaeh, **B. Earl Wells**, *Proceedings of the 28th IEEE Southeastern Symposium on System Theory*, March 31-April 2, 1996.

[C.11] "An Improved Heuristic Model for Task Allocation in Distributed Computing Sys- tems", A. Abdelmageed Elsadek and **B. Earl Wells**, *Proceedings of the International Con- ference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 95)*, Athens, GA, pp. 187-196, November 3-4 1995.

[C.10] "The Simultaneous Optical Multiprocessor Exchange Bus" J. Kulick, W. E. Cohen, C. Katsinis, **E. Wells**, A. Thomsen, R. K. Gaede, R. G. Lindquist, G. P. Nordin, M. Abush- agur, D. Shen, *Proceedings of the Second International Conference on Massively*

Parallel Processing Using Optical Interconnections, San Antonio TX, pp. 336-344, October 1995.

[C.9] "A New Measure for Accessibility" J. Neggers, **B. E. Wells**, presentation made at the *7th Cumberland Conference on Graph Theory and Computing*, The University of Alabama in Huntsville AL, May 12, 1994.

[C.8] "A Parallel Task Allocation Methodology for Non-Buffered Message-Passing Envi- ronments, "Proceedings *of IEEE Southeastcon 93"*, **B. Earl Wells**, D. J. Jackson, and C. C. Carroll, fully refereed paper category (8 pages), April 1993.

[C.7] "Analysis of Random Digraph Generation Techniques for use in the Evaluation of Parallel-Processing Static Task Allocation Heuristics," **B. Earl Wells** and Joseph Neggers, *Proceedings of 25th IEEE Southeastern Symposium on System Theory*, pp. 477-481, 1993.

[C.6] "An Augmented Approach to Task Allocation: Combining Simulated Annealing with List-Based Heuristics", **B. Earl Wells** and C. C. Carroll, *Proceedings of the Euromicro Workshop on Parallel and Distributed Processing*, Gran Canaria, pp. 333-338, January 1993.

Conferences (continued):

[C.5] "An Automated Post-Allocation Translator for Parallel Dynamic System Simula- tion," *Proceedings of IEEE Southeastcon '92*, **B. Earl Wells**, D. McGhee and C. C. Carroll, pp. 327-330, April 1992.

[C.4] "Parallel Simulation of a Space Shuttle Main Rocket Engine," *Proceedings of the Twentieth Annual Pittsburgh Conference on Modeling and Simulation*, **B. Earl Wells** and C. C.

Carroll, Vol. 20, Part 2. pp. 603-607, 1990.

[C.3] "Applying Parallel Block Predictor-Corrector Methods to a Space Shuttle Main Rocket Engine Simulation", *Proceedings of IEEE Southeastcon '90*, **B. Earl Wells** and C. C. Carroll, pp. 614-617, April 1990.

[C.2] "Simulation of a Space Shuttle Main Rocket Engine in a Multi-Transputer Environ- ment", *Proceedings of ISMM International Symposium on Computer Applications in Design, Simulation and Analysis*, **B. Earl Wells** and C. C. Carrol, pp. 69-73l, March 1990.

[C.1] "Parallel Methods for Real-Time Simulation of Continuous Systems," *Proceedings of IEEE Southeastcon '89*, **B. Earl Wells** and C. C. Carroll, Vol. 2, pp. 505-510, 1989.

***Funded Research**:**

"Common Hardware-in-the-Ioop Simulation Development," **B. Earl Wells**, PI, Task Scope, Development high speed, low latency data interfaces between FPGA boards and data storage devices, Torch Technologies/Army AMSRD, **Award Period 12/15/2011 -- 9/ 30/2012**. Funding $32.733.46.

"Simulation Development and Analysis of Air and Missile Defense Systems," TI A01110147, R3 428-1, **B. Earl Wells**, PI, Task Scope, Development high speed, low latency data interfaces between FPGA boards and data storage devices, Torch Technologies/Army AMSRD, **Award Period 7/1/2011 -- 2/28/2012**. Funding $48,166.60.

"Implementing Model Based Design techniques in Multi-core applications". Jeff Kulick, PI, **B. Earl Wells** (team member) Science Applications International Corporation and Soft- ware Engineering Directorate. May 2010 - November 2010. Funding Amount $39,824.

"Model Based Design using High Level Abstractions that can be Exploited by Modern CAD Tools - Development of a Simulink to Mentor Catapult C Translator. B. Earl Wells (team member). Science Applications International Corporation and Software Engineering Directorate. February 2009 - August 2009. Funding 32,549.

"Parallel Particle-in-Cell code Development for the Kinetic Simulation of Astrophysical Plasmas Affecting Magnetic Reconnection," Nagendra Singh, B. Earl Wells, UAH ECE Funded Research Enhancement Program, AY 2007/2008, Funding $31,000.

"Parallel Particle-in-Cell Code Development for the Kinetic Simulation of Astrophysical Plasmas Affecting Magnetic Reconnection," **B. Earl Wells**, Nagendra Singh, UAH College of Engineering Research Enhancement Award, Funding $27,000. **Award Period 10/2007 - 08/2008.**

"Development of Parallel Program Implementations for Electromagnetic Simulations," **B. Earl Wells**, NASA/USRA Consulting Contract NCC8-259 3491.03.05.01.06, Funding $16,250. **Award Period 6/1/05-12/31/05**.

* PI listed first followed by Co-PI(s)

Funded Research (continued):*

"Development of New Parallel Reconfigurable Processing Techniques for Aerospace Applications," NASA Sabbatical Research IPA-023, Marshall Space Flight Center, **B. Earl Wells**, Funding $29,931, **Award Period 8/18/03--5/21/04**.

"Intelligent Control for Future Deployable Autonomous

Distributed Sensor Systems," **B. Earl Wells**, Office of Naval Research DEPSCOR Program, (project with Thomas Jan- nett, and Murat Tanik, University of Alabama at Birmingham with Dr. Jannett being overall project PI), Funding (UAH) $138,712, **Award Period 6/1/03 -- 5/31/06**.

"Microphysica of Plasma Processes Dissipating Inertial Alfven Waves," Nagendra Singh, **B. Earl Wells**, NASA Headquarters, Funding $335,122, **Award Period 6/1/03 -- 5/30/06**.

"Auroral Potential Structures in the Upward Current Region," Nagendra Singh, **B. Earl Wells** (Teaming Partner), NASA, Funding $264,013, **Award Period 3/15/03 -- 3/14/05**.

"Mesoscale Kinetic Simulations of the Potential Structures in the Auroral Return Current Plasma, Nagendra Singh, **B. Earl Wells**, National Science Foundation, NSF ATM- 0206669, Funding $282,579, **Award Period 7/1/2002 -- 6/30/2005**.

"Reconfigurable Computing Research and Design," **B. Earl Wells**, NASA, Funding $77,994. **Award Period 9/9/99--9/8/00.**

"Three-Dimensional Kinetic Simulation of Excitation and Nonlinear Evolution of Lower Hybrid and VLF Waves in Filamentary Electron Beams in the Topside Ionosphere," Nagendra Singh, **B. Earl Wells**, National Science Foundation, Funding $229,105, **Award Period 4/1/99 --10/31/02**.

"Integrated Research Environment for Intermeshed Optoelectronics," NSF 97-374 EPSCoR Infrastructure Development Proposal, G. P. Nordin, S. T. Kowel, W. E.Cohen, R. L. Fork , R. K. Gaede, J. H. Kulick, R. G. Lindquist, D. Shen, **B. E. Wells**, National Science Founda- tion, Funding $1,843,000, **Award Period 5/98 -- 5/01**.

"CISE Research Instrumentation: Infrastructure to Support Accurate Performance Measure- ments of Multithreaded

Programs," W. Cohen, **B. E. Wells**, K. Kavi, National Science Foundation, Funding $55,000, **Award Period 2/15/98--1/31/99**.

"Model Based Design using High Level Abstractions that can be Exploited by Modern CAD Tools - Development of a Simulink to Mentor Catapult C Translator". Jeff Kulick, et. al. **B. Earl Wells** (team member). Science Applications International Corporation and Soft- ware Engineering Directorate. Funding ~$40,000. **Award Period 4/2009--9/2010.**

"Real-Time Embedded Diagnostics and Self-healing Analysis," **B. Earl Wells**, Contract No. DAAH01-97-D-R005 D.O. 5, U.S. Army Aviation and Missile Command, Funding $24,834, **Award Period 5/98 -- 12/98**.

"Technique and Development of Radiation Hardened Digital Signal Processor," Mark Maier, **B. Earl Wells**, Phase I STTR Space Electronics Corporation/Ballistic Defence Orga- nization, Funding $19,982, **Award Period 10/2/97 to 7/31/99**.

"Continued Research on Excitation of Nonlinear Propagation of Lower Hybrid Waves in Auroral Plasma," Nagendra Singh, **B. Earl Wells**, NASA, Funding $39,000, **Awarded Period 5/97 -- 4/98**.

* PI listed first followed by Co-PI(s)

Funded Research (continued):*

"Simulating an Advanced Tether Dynamics Problem on a Network of Heterogeneous Workstations" in support of NASA Phase I SBIR No. 96-1 07.04-8798 "Advanced Tether Dynamics Simulation," **B. Earl Wells**, Control Dynamics Corporation,

Funding -- $14,411 **Award Date 4/10/97**.

"Development and Implementation of Effective Fault-Tolerant Scheduling Methodologies for Distributed Hard Real-Time Processing of Large-Scale Applications," **B. Earl Wells**, U.S. Army Missile Command, Funding -- $43,859 **Awarded 12/12/96**.

"Research and Development of Components of the Students for the Exploration of Space Satellite (SEDSAT) for the Small Expendable Deployer System (SEDS) Project Office", **B. E. Wells**, M. W. Maier, NASA Marshall, Funding -- $36,223 **Awarded 10/1/95**.

"Analysis of Heuristic Static Task Allocation Methodologies as Applied to Create Large- Scale Highly-Parallel Simulations," **B. Earl Wells**, UAH Research Institute Mini-Grant Funding -- $1,895 **Awarded 1/1/93**.

Research Fellowships:

Awarded a NASA/ASEE Faculty Fellowship in Aeronautics and Space Research, Marshall Space Flight Center, **10 Week Stipend Support** (Summer 2002).

Awarded a NASA/ASEE Summer Faculty Fellowship in Aeronautics and Space Research, Marshall Space Flight Center, **12 Week Stipend Support** (Summer 1996).

Awarded a NASA/ASEE Summer Faculty Fellowship in Aeronautics and Space Research, Marshall Space Flight Center, **10 Week Stipend Support** (Summer 1995).

Awarded Graduate Council Research Fellowship, Graduate School, The University of Ala- bama (Tuscaloosa) (1990-1991 academic year).

Awarded Graduate Council Research Fellowship, Graduate School, The University of Ala- bama (Tuscaloosa) (1989-1990

academic year).

* PI listed first followed by Co-PI(s)

16/19

Formal Presentations:

[Pr.3] “Parallel, Reconfigurable, and General Purpose GPU Accelerated Computing at UAH,” Invited Colloquia Presentation given to the Electrical Engineering Computer Sci- ence Department Faculty at Alabama A&M University, Huntsville, Alabama April 3, 2015.

[Pr.2] “Graduate Educational and Research Experiences at UAH,” **B. Earl Wells**, Invited Presentation to the Electrical and Computer Engineering Faculty of Boise State Univer- sity, March 22, 2007.

[Pr.1] Invited Presenter -- 2005 Chief Scientist Lecture Series (Advanced Computing Architectures) Air Force Research Laboratory, “Reconfigurable Hardware and Hybrid Architecture approaches for solving Evolutionary Computing Optimization Problems and performing Process Scheduling,” **B. Earl Wells**, Rome NY, July 19, 2005.

Awards: Awarded the ***IEEE Outstanding Educator Award***, Huntsville Section, February 23, 2013.

Co-author winner of one of three *Best Paper* Awards (out of 169 papers) presented at the *International Symposium of Performance Evaluation of Computer and Telecommunications Systems* (SPECTS'05). The paper was entitled "Microarchitecture Support for the Dynamic Scheduling of Task Systems with Data and Control Dependencies on Reconfigurable Architectures", Zexin Pan, **B. Earl Wells**, and Jaunjo Nogurera.

Best Paper of Session Award at the 20th Digital Avionics Systems Conference, Daytona Beach, FL. October 14-18, 2001. Paper title: "On the Use of Distributed Reconfigurable Hardware in Launch Control Avionics," **B. Earl Wells**, Sin Ming Loo.

Co-Recipient of the *D. W. Burlage Award* for Outstanding Research in Computer Architecture, University of Alabama -- Tuscaloosa -- ECE Department, College of Engineering 1990.

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Service Activities

Professional Service Activities:

•Technical Reviewer for the Journal of Supercomputers, 2012-2013.

•Panel Reviewer for the Small Business Innovation Research/Small Business Technology Transfer Panel National Institute of Health, April 1-2 and April 20-21, 2010.

•Technical Paper Reviewer 2010 IEEE Southeastern Symposium on System Theory.

• Text book reviewer McGraw-Hill, February 2010

• Technical Paper Reviewer for the Reconfigurable Systems Summer Institute 2007, National Center for Supercomputing Applications, Urbana, Illinois, July 17-20, 2007. •Reviewer for the *IEEE Transactions on Education*, August 2007.

• Program Committee Member/ Technical Reviewer for the 2007 International Conference on Embedded Software and Systems (ICESS), Embedded Hardware Track.

• General Conference Chair, International Society for Computers

and Their Applications (PDCS-2006), San Francisco, CA, September 20-22, 2006.

- Technical Reviewer for the journal *Computing Letters* (CoLe), April 2006.

- Program Committee Member/Technical Paper Reviewer: 21st International Conference on Computers and Their Applications (CATA-2006), Seattle Washington, March 2006.

- Technical Reviewer for the Deep Space Test Bed Project, Avionics, Critical Design Review, NASA MSFC, March 2004

- Member of Program Committee/Technical Paper Reviewer: 16th International Conference on Parallel and Distributed Computing Systems (PDCS-2003), Reno, Nevada, USA (August 13 - 15, 2003).

- Session Chair: Session TA1-1: Computer Systems II; Software Session, for the Thirty- Fourth Southeastern Symposium on System Theory Conference (SSST2002), Huntsville, Alabama (March18-19, 2002).

- Supervising Proctor for Fundamentals of Engineering Examination, State Board of Registration for Professional Engineers and Land Surveyors, Huntsville, AL (October 27, 2001).

- Technical paper reviewer for the 4th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP2000), Hong Kong (Dec. 11-14, 2000).

- Panel reviewer for National Science Foundation Undergraduate

Education Curriculum and Laboratory Improvement program (CILI), (Committee Member 1998/Panel Chair 1999).

- Technical paper reviewer for *The International Journal of Computers and Their Applications* (1996/1997/2007).

- Technical paper reviewer for The Journal of Supercomputing (1997).

- Technical referee for the 20th Army Science Conference -- High-performance Computing and Simulation Section (1996).

- Instructor for Fundamentals of Engineering Examination for the Continuing Education Department at UAH (1996,1997).

- Supervising Proctor for Engineers-in-Training Examination, State Board of Registration for Professional Engineers and Land Surveyors, Huntsville, AL (Spring Exam 1996).

- Judge for the Research and Technical Paper Competition for the Science and Engineering Apprentice Program, U.S. Army Missile Command (August 3, 1995).

- Session Chair: Models, Theories, and Methodologies Session, Conference on Parallel and Distributed Techniques and Applications, Athens GA (1995).

University Service Activities:

•Member of EngineeringFaculty Awards Selection Committee (2015) •Member of Engineering Executive Council (May 2014-- present) •Member of Faculty Senate (2014-- present) •ABET ECE Program Advisory Board Member (2003, 2006)

•ABET ECE Industrial Advisory Board Member (2006/2007)

•COE Curriculum Assessment Team (CAT) Member (2006 -- 2008)

•COE Engineering Open House Committee Member (2006)

•Member UAH-UAB Computer Engineering Shared Ph.D. Coordinating Board (2001 -- present)

•Computer Engineering Faculty Committee (1992 - 2006 -- Committee Chair 2006 -- present)

•Member of the College of Engineering Professional Licenser Committee (2001 -- 2003) •Departmental Faculty Reappointment Committee (1999, 2003, 2005, 2006) •Departmental Laboratory Manager Search Committee (Chair 2005) •Full member of the Graduate Faculty (1994 -- present) [Associate Member 1992-1994] •Served on 148 individual Masters and Ph.D. graduate student committees (1992- present) •Mentoring Instructor, UAH Integrated Product Team (1996, 1998-2003, 2006)

•Judge in UAH Co-op of the Year Competition (2002) •Member of the College of Engineering Curriculum Assessment Team (2006-present) •Member of the College of Engineering Advising Committee (1993) •Member of Faculty Senate (1997-99)

Member Academic Affairs Committee (1997-98)

Member of Personnel Committee (1998-99)

•Member of the ECE Graduate Affairs Committee (1992-94, 1995-99)

•Member of the ECE Planning Committee (1998-1999)

•Member of the Engineering Curriculum Committee (1995-96)

•Member of the MAE Laboratory Committee (1995)

•Member of College of Engineering Brian Helmrich Scholarship Committee (1993-94)

•Served as a Graduate School Observer for Ph.D. Qualifying Exams for the Physics, Com- puter Science, English, and Mathematics Departments. (1994-present)

•Composed and Graded Approximately 10 Departmental Ph.D. Preliminary Examinations

•Faculty Advisor for UAH student chapter of the National Society of Professional Engineers (1992-1997)

Professional Organizations:

Member Institute of Electrical and Electronics Engineers (IEEE) Member Association for Computing Machinery, ACM Order of the Engineer (Link 179)

Additional Technical Licenses:

Holder of a U.S. General Radio Telephone License with Radar Endorsement Holder of Amateur Radio Extra Class License, KZ4W